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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Complete if Known			
Application Number		09/531,633	
Filing Date		03-21-2000	
First Named Inventor		Zhe Li	
Group Art Unit		2787	
Examiner Name			
Sheet	1	of	2	Attorney Docket Number		

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	U.S. Patent Document Number	Kind Code[2] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
EG	1	5,032,988		F. J. van der Linden	07-16-1991	
	2	5,243,538		O. Okuzawa et al.	09-07-1993	
	3	5,276,897		G. M. N. Stalmarck	01-04-1994	
	4	5,526,514		D. Pradham and W. Kunz	06-11-1996	
	5	5,748,486		P. Ashar and C. Cheong	05-05-1998	
	6	5,946,481		R. P. Kurshan and C. M. Roman	08-31-1999	
EG	7	5,949,691		H. Kurosaka et al.	09-07-1999	

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Office[3]	Number[4]	Kind Code[5] (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature	ED GARCIA-OTERO	Date Considered	6/18/03

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[1] Unique citation designation number. [2] See attached Kinds of U.S. Patent Documents. [3] Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6] Applicant is to place a check mark here if English language Translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Application Number		09/531,633	
Filing Date		03-21-2000	
First Named Inventor		Zhe Li	
Group Art Unit		2787	
Examiner Name			
Attorney Docket Number			

Sheet	2	of	2

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
EG	8	R. E. Bryant, "Symbolic Boolean Manipulation With Ordered Binary Decision Diagrams", ACM Computing Surveys, Vol. 24, No. 3, September 1992, pp. 293-318.	
	9	J. R. Burch, V. Singhal, "Tight Integration of Combinational Verification Methods", IEEE/ACM International Conference on Computer Aided Design Digest of Technical Papers, November 1998, IEEE, Piscataway, NJ, USA, pp. 570-576.	
	10	C. A. J. van Eijk, "A BDD Based Verification Method for Large Synthesized Circuits", INTEGRATION, the VLSI Journal, Vol. 23, No. 2, November 1997, pp. 131-149.	
	11	J. Jain et al., "A Survey of Techniques for Formal Verification of Combinational Circuits", Proceedings of IEEE International Conference on Computer Design: VLSI in Computers and Processors, October 1997, IEEE, Piscataway, NJ, USA, pp. 445-454.	
	12	J. P. Marques-Silva, K. A. Sakallah, "Boolean Satisfiability in Electronic Design Automation", Proceedings of 37th Design Automation Conference, June 2000, IEEE, Piscataway, NJ, USA, pp. 657-662.	
EG	13	S. Woods, G. Casinovi, "Efficient Solution of Systems of Boolean Equations", IEEE/ACM International Conference on Computer Aided Design Digest of Technical Papers, November 1996, IEEE, Piscataway, NJ, USA.	

Examiner Signature	EP GARCIA-OTERO	Date Considered	

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